IN THE CLAIMS:

This listing of claims will replace all prior versions, and listing of claims, in the Application.

Listing of claims:

1.   (Currently amended) A method of reducing power consumption in an integrated circuit communication link having a logic circuitry, the logic circuitry including supply-voltage-critical logic circuitry and non-supply-voltage-critical logic circuitry, the method comprising the steps of:

synthesizing the integrated circuit to identify the supply-voltage-critical logic circuitry;

isolating the supply-voltage-critical logic circuitry from the non-supply-voltage-critical logic circuitry, the supply-voltage-critical logic circuitry being driven by a first supply voltage and the non-supply-voltage-critical logic circuitry being driven by a second supply voltage, the first supply voltage being greater than the second supply voltage wherein the first supply voltage is supplied to the communication link and wherein the first supply voltage is used to generate the second supply voltage;

embedding a voltage regulator in the communication link for supplying the second voltage; and

selectively interfacing the supply-voltage-critical logic circuitry with the non-supply-voltage-critical logic circuitry using level shifters wherein the selectively interfacing step includes the step of selecting a minimal number of points at which the supply-voltage-critical logic circuitry interfaces with the non-supply-voltage-critical logic circuitry.

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2-4.   Canceled.

5.   (Currently amended) The method of Claim [[4]] 1 wherein a level shifter is
used at each interfacing point.

6.   (Original) The method of Claim 5 wherein the communication link is on a
chip, the chip having a multiplicity of communication links, a plurality of the
multiplicity of the communication links sharing the embedded voltage
regulator.

7–17. Canceled.

18-20. Canceled.